Low Temperature Through-Wafer Reactive Ion Etching for MEMS

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***Abstract*—This paper presents the results of experimental work on a low temperature through-wafer reactive ion etching (RIE) technique obtained in the course of development of a process that can be used in small sample processing for microelectromechanical systems (MEMS). Low temperature RIE are a crucial step for many dry MEMS fabrication processes, where can be used to fabricate silicon vias, trenches, and to perform dry release of membranes and other devices. The through-wafer etch developed here can be used also to separate fabricated devices, especially when it is desirable to produce non-rectangular shapes, which cannot be cut using a dicing saw. The presented process works with large silicon wafers as well as with small samples. In this work we developed a method which allows for stabilization of the sample temperature at the correct level during the entire process, which allows through wafer etch of thick silicon samples. The results obtained indicate that there is no universal process suited to all applications. Here we present three different recipes suitable for various applications.**

***Index Terms*—Low temperature etching, Microelectromechanical systems, Plasma process, Silicon**

I. Introduction

Plasma reactive ion etching is a fundamental techniques used in current microelectronics (IC) and micro-fabrication facilities. It is widely used to create through silicon vias for 3D packaging technology [1], silicon on insulator (SOI) waveguides [2] and dry release of MEMS structures [3].

Deep reactive ion etching in silicon is generally performed with two different processes. The Bosch process [4]–[6] is the most popular, and can be executed at room temperature. It consists of two stages: etch and passivation. First, an isotropic silicon etch in SF_6 plasma is performed, followed by a passivation polymer deposition step, in which one of following gases C_4F_8, C_3F_6, $(C_3F_6)_2$ or CHF_3 is used. Both steps are looped in short cycles. During the process a thin passivation layer (about 20 nm) is deposited on the sidewalls and, after etching, this layer needs to be removed in a separate process. This is the biggest disadvantage of the Bosch process. The second commonly used process, reactive ion etching at low temperatures [7], uses a different passivation deposition mechanism. This process is conducted at low temperatures, in which a SiO_xF_y passivation layer is deposited on the sidewalls [8]. This process allows smooth sidewalls to be created, but it is much more difficult to control and very sensitive to temperature changes. An additional advantage of the process is that the passivation layer is desorbed during the heating of the sample [8], a feature that can be important for the fabrication of microelectromechanical devices (MEMS).

The goal of this experimental work was to develop a method which allows the deep etching of small samples.

II. Experiment

The experiments were performed using a Plasmalab 100 system from Oxford Instruments. In this system a four inch wafer is mechanically clamped to a liquid nitrogen cooled table. To allow proper thermal contact between table and wafer, helium backing was introduced. During the conducted experiments this helium backing pressure was set at constant value of 1.33 kPa.

A. Carrier wafer

The simplest solution is to use a silicon carrier wafer. This is an acceptable solution for some processes, but is very inefficient for deep etching. There is the need to use a carrier wafer much thicker than the etched features, which can be difficult and expensive for 300 µm or deeper through wafer etches. In addition, a large amount of etched silicon could have a negative impact on the etch rate. Consequently, it was decided to use a four inch sapphire substrate instead, as sapphire is highly resistant to a SF_6/O_2 plasma etch at low temperatures.

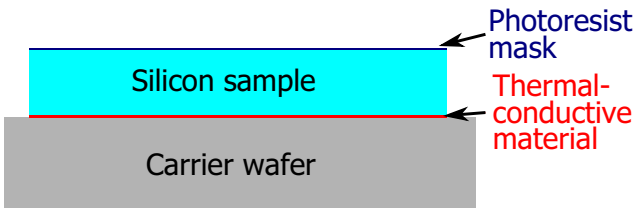

Fig. 1. Sample on carrier wafer

B. Thermal contact between sample and a carrier wafer

In order to enhance thermal conduction, thermally conductive material was introduced between the etched sample and the carrier wafer (Fig. 1). Initially wax was used, as this is a popular material for mounting small samples on carrier wafers for plasma etching. This popularity is due to its ease of use and that it reduces the level of contamination introduced into the chamber. Unfortunately even a thin layer of wax acted as a thermally insulating layer and made it impossible to maintain the correct sample temperature during processing. After the initial unsuccessful tests with wax, it was decided to use a mechanical vacuum pump oil - Solvay Solexis Fomblin Inert PFPE Fluid. A thin layer of this oil was introduced between the sample and carrier wafer to provide proper thermal contact, and was shown to give good results.

C. Photoresist mask

Another important factor was the proper photoresist pattern preparation process to avoid photoresist cracking. We used AZ2070 photoresist, with a standard thickness of 3.5 µm. It was important to achieve sidewalls as straight as possible in the prepared pattern. Any undercut produced during the lithography process led to photoresist cracking during the cooling stage (Fig. 2). To avoid cracking the masks were

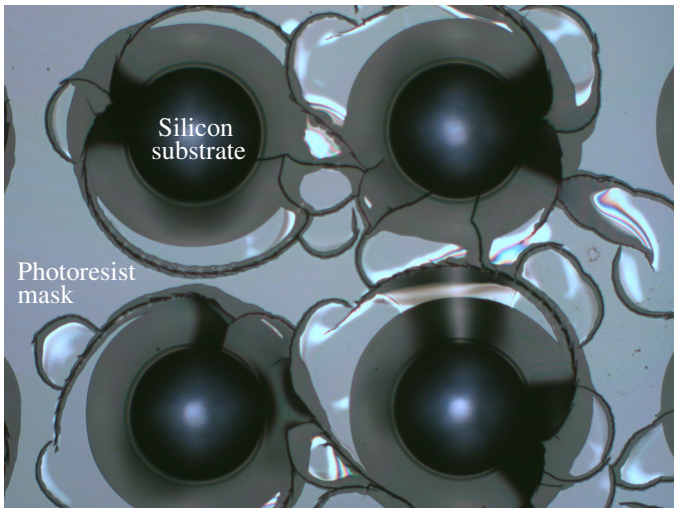

Fig. 2. Cracked photoresist mask with circular features on silicon

hard baked after lithography. Hard baking was performed on a hotplate at 113 °C for 30 minutes.

D. Etching recipes

During this work three different dry etching recipes were developed, each for different application. Each recipe consists of an initial 40 minute sample cooling step, followed by a plasma strike procedure (Fig. 3) and finally the silicon etching step.

In Recipe 1, the silicon etching step includes only one operation, in which the O_2/SF_6 ratio was equal to 13.4% (O_2 flow 10.7 sccm, SF_6 flow 80 sccm). Etching was performed in two

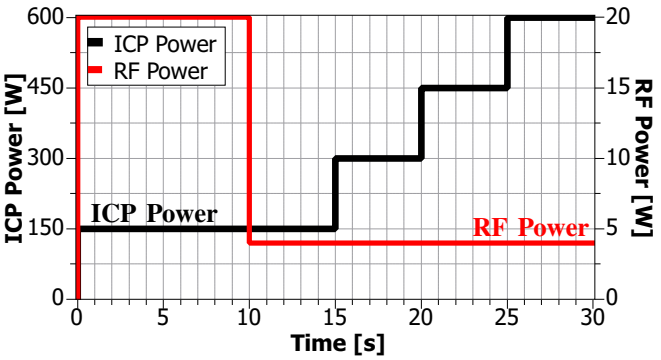

Fig. 3. Plasma strike power sequence

steps, 10 minutes each, separated by a 10 minute sample cooling period.

Recipe 2 is similar to Recipe 1, however the O_2/SF_6 ratio was changed to 9.2% (O_2 flow 10.7 sccm, SF_6 flow 116 sccm).

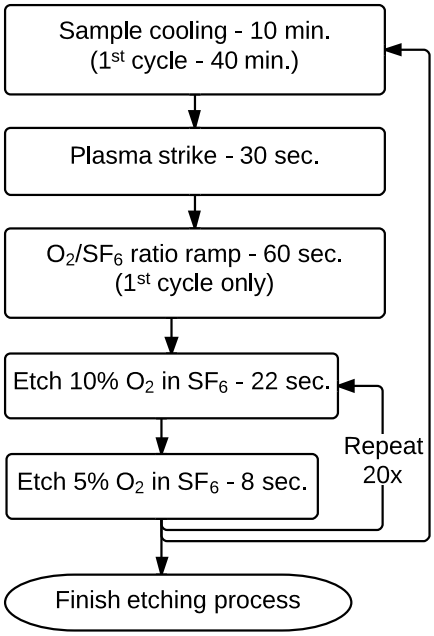

Fig. 4. Recipe 3 - flow chart

Recipe 3 (Fig. 4) is completely different to the first two processes. At the beginning, an under-etch reduction step was introduced. During the first minute of this process, the O_2/SF_6 ratio was ramped, starting from pure oxygen plasma up to the final ratio of 10% O_2 in the SF_6 in order to reduce under etch [9]. Following this, the etching is conducted in a repetitive two stage cycle [10]: In the first stage, the O_2/SF_6 ratio was set to 10% (O_2 flow 10.7 sccm, SF_6 flow 106 sccm) for 22 seconds. This stage, except etching, is designed to generate a significant passivation layer. However, it also causes a build up of black silicon on the bottom of features. Second, a much lower O_2/SF_6 ratio of 5% is used (O_2 flow 5.7 sccm, SF_6 flow 116 sccm) and run for 8 seconds. This step, except etching, is

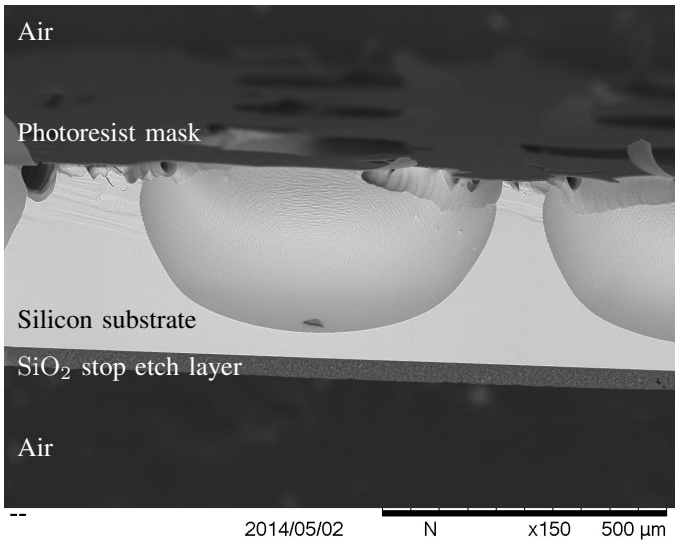

Fig. 5. Etching at too high sample temperature results in isotropic profile

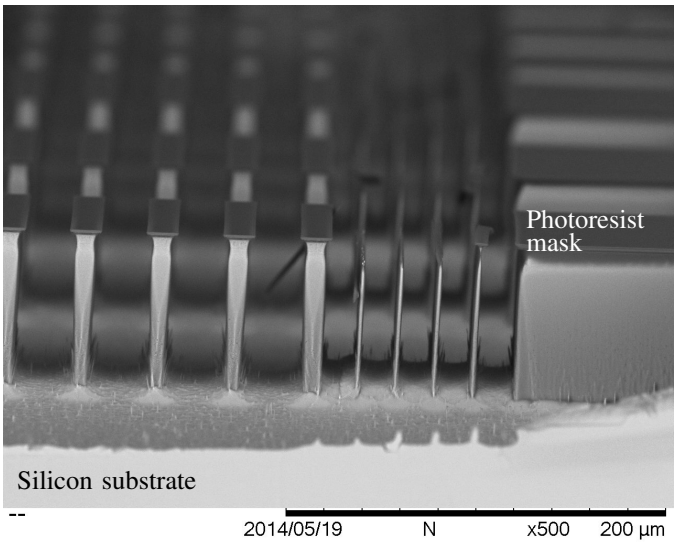

Fig. 7. Recipe 1 - fabricated columns. Note the initial under etch

designed to remove black silicon built up in the first step.

Other parameters used during all processes were constant: temperature $-100\,^{\circ}\mathrm{C}$, pressure $2\,\mathrm{Pa}$, helium backing pressure $1.33\,\mathrm{kPa}$, RF power $4\,\mathrm{W}$ and ICP power $600\,\mathrm{W}$.

III. Results

Fig. 5 shows isotropic etch profile obtained with Recipe 1 without the 40 minute cooling step. Similar results were obtained for a sample attached to the carrier wafer using wax as thermal interface material.

Next, the same recipe was used, but with the addition of the 40 minute cooling step to assure sample reaching low temperature ($-100\,^{\circ}\mathrm{C}$). A good etching profile was obtained (Fig. 6, 7), but only for a depth of about $100\,\mu\mathrm{m}$, where the process was stopped due to extensive formation of black silicon. In addition, a strong influence of the feature size on etching speed was observed (Fig. 6).

Following further investigation, the oxygen content in the SF_6/O_2 plasma was reduced (Recipe 2) which allowed etching almost through $300\,\mu\mathrm{m}$ thick silicon wafer. Recipe 2 etches up to depth of about $290\,\mu\mathrm{m}$ and then stops due to black silicon formation at the bottom. Consequently, it cannot be used to release membranes or etching deeper than $290\,\mu\mathrm{m}$. The biggest disadvantages of Recipe 2 are rough sidewalls of the etched features, due to black silicon formation during the process, and the inability to create clean of black silicon membranes (Fig. 8).

Recipe 3 solved all the problems of the previous two. It allows fabrication of deep trenches and release of mem-

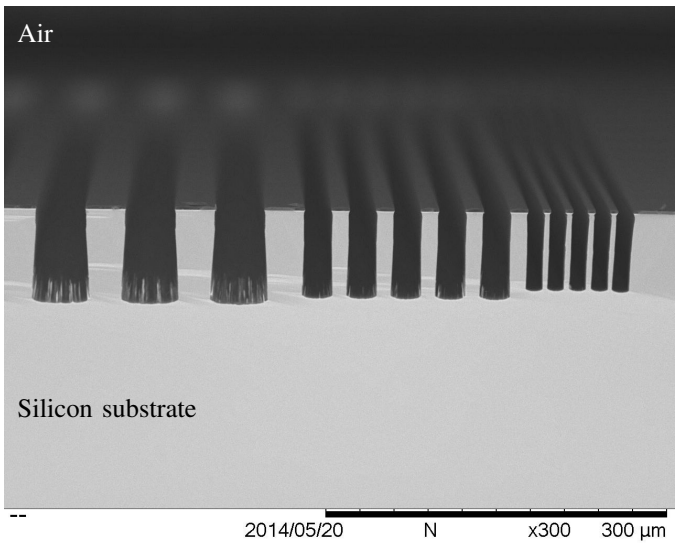

Fig. 6. Recipe 1 - fabricated trenches

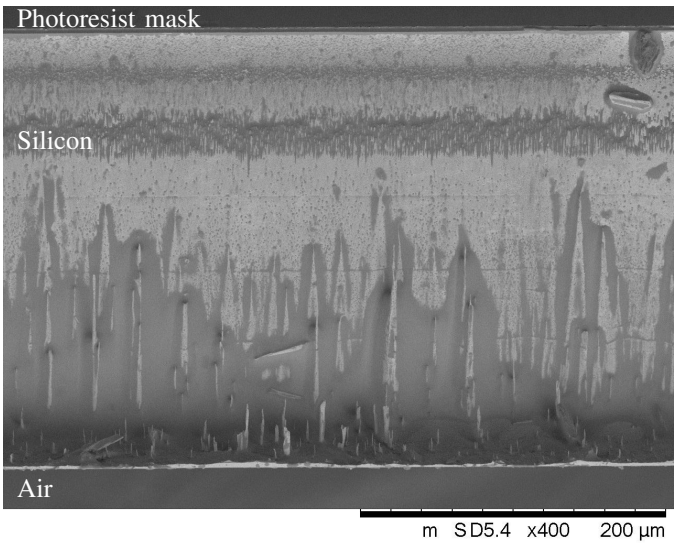

Fig. 8. SEM image of trench wall etched using Recipe 2

branes deposited on 300 µm and thicker silicon substrates. Fig. 9 shows walls of etched trenches in 300 µm thick silicon wafer with SiO_2 layer deposited at the bottom. The second etching stage in this recipe, with the O_2/SF_6 ratio of 5%, removes the produced black silicon, and allows very deep etching (more than 300 µm). A small, 20 µm under etch, at the beginning of the process is still evident. It can be compensated by extending the initial passivation step with the O_2/SF_6 ratio ramp. The slope of the walls was found to be about 5°, which is an satisfactory result.

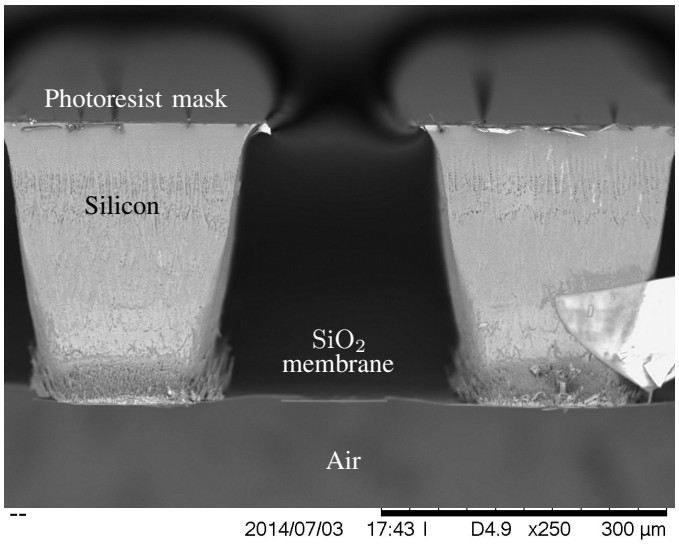

Fig. 9. SEM image of 300 µm deep etch with released SiO_2 membrane

IV. Conclusion

We presented three recipes for low temperature reactive ion etching of silicon. Each recipe is applicable for different processes depending on required parameters of etched structure. Recipe 1 produce good etching profile, but only for a depth of about 100 µm. Recipe 2 etches up to depth of about 290 µm, however produces rough sidewalls. Most advanced Recipe 3 allows etching in excess of 300 µm depth with very straight sidewalls. All of them can be used on very small silicon samples as well as on large silicon wafers.

Future process adjustments will focus on the elimination of under etch, which should be solved by extending the passivation step at the beginning of the process. Also, the sapphire carrier wafer may be able to be replaced by a silicon substrate covered with a thin layer of aluminium oxide. This should improve thermal parameters and allow shorter cooling periods.

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