# Capturing the Impulse Response of a Second Order System

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***Abstract*—The impulse response of a system is of great significance when analysing a system's properties. Due to the short time scales involved in some cases, capturing this transient response requires a high degree of timing accuracy. This paper discusses the techniques used in designing a data acquisition system for initiating and recording the impulse response of a second order system. Consisting of an ADC, input buffer, FPGA, and GUI, the system can be used to analyse a range of system responses on nanosecond time scales.**

***Index Terms*—Data Acquisition; Impulse Response; Micro-Electro-Mechanical Systems; Resonant Frequency**

## I. Introduction

The impulse response of a system is a powerful tool that can provide a wealth of information on the system under consideration. When exposed to a brief input signal, an impulse, a system will react in a characteristic way know as its impulse response. This concept is regularly used in many applications as a method of characterising system properties, such as a system's transfer function in the field of control systems. Of particular interest is the impulse response of Micro-Electro-Mechanical Systems (MEMS). It is well know that a mechanical structure will vibrate at its resonant frequencies when exposed to an impulse exciting force, allowing these properties to be easily measured. Determining the resonant frequency of a MEMS structure is crucial to its operation and, as such, methods used in measuring this must provide a high level of accuracy.

The impulse response of many structures can be modelled using an underdamped second order transient response [1]. For a structure with a resonant frequency $\omega_0$, damping ratio $\zeta$, and spring constant $k$, the second order system response can be modelled by,

$$\ddot{x} + 2\zeta\omega_0\dot{x} + {\omega_0}^2 x = \frac{{\omega_0}^2}{k}F(t), \tag{1}$$

where $F(t)$ is an impulse of magnitude $F$. As can be seen in Figure 1, the structure's motion must be captured in the brief window of time following the impulse, before the vibration decays back to its resting state. This highlights the necessity for a data acquisition system with a high degree of control over the timing of the impulse excitement and subsequent sampling of the structure's position.

In most applications, a true impulse of infinitely short duration cannot be realised, resulting in the impulse response being approximated by a finite pulse.

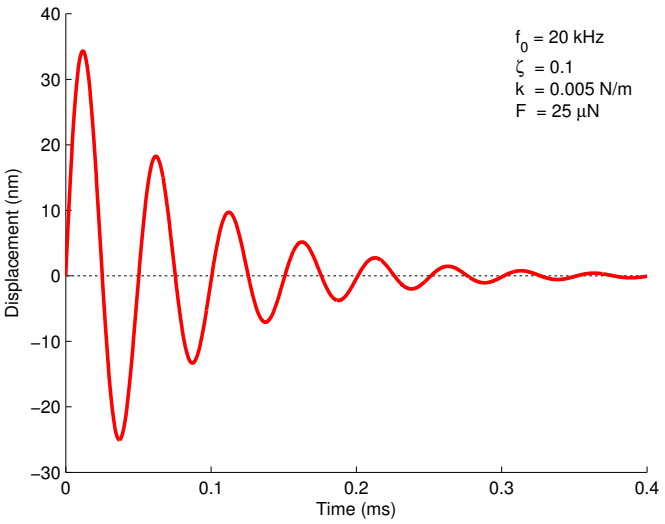


Fig. 1. The impulse response of a second order system, subjected to a 25 $\mu$N impulse. The structure has a resonant frequency of 20 kHz, a damping ratio of 0.1, and a spring constant of 0.005 N/m

## II. Data Acquisition System Design

In order to capture and analyse the impulse response of a MEMS structure, a data acquisition system has been designed to initiate an impulse excitement and begin sampling a position-sensitive signal at set intervals. The design features a Field Programmable Gate Array (FPGA), Analog-to-Digital Converter (ADC), buffer amplifier, and a computer interface. These components were selected to enable precision timing and accuracy within the design, allowing samples to be captured, processed, and then displayed in near real-time. The computer interface also presents a number of modifiable parameters, giving the user full control over the device operation.

### A. Analog-to-Digital Converter

The ADC used in the design is a MAX1308 by Maxim®, featuring simultaneous channel sampling rates of up to 1 MHz and a Signal-to-Noise Ratio (SNR) of 71 dB [2]. This 12-bit ADC operates using a standard interface, where a conversion is initiated and then read via a parallel 12-bit bus once the conversion result is ready. Given that impulse response signal to be measured is confined to within $\pm$5 V, the MAX1308 enables full use of this dynamic range.

When implemented into the design, a MAX1308 Evaluation Kit was used to streamline the design of the various inter-

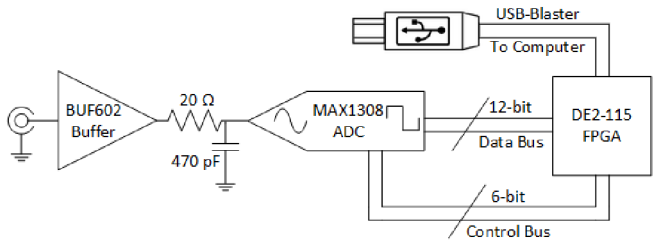


Fig. 2. A simplified circuit diagram of the data acquisition showing the interconnection between each of the components.

connects necessary for the ADC's operation [3]. While the evaluation kit offers four MAX4351 op-amps as buffers, their common-mode input range only extends to within 2.25 V of the positive supply rail [4]. The high degree of non-linearity outside this range impedes the use of the full input range, rendering them unsuitable for the design. Instead, a BUF602 high-speed buffer by Texas Instruments® is used to drive the ADC inputs. The larger common-mode range on this device allows the full ADC input range to be used while still exhibiting linear behaviour [5].

### B. FPGA

At the heart of this system is the FPGA, a semiconductor device that can be programmed by the user. Any realisable logical function can be designed and implemented using hardware description language (HDL), resulting in a device that is ideal for tasks requiring a high degree of timing precision and functionality. The designed system uses a DE2-115 Development and Education Board from Terasic®, featuring a Cyclone® IV FPGA by Altera®. The large selection of available I/O, including a USB port and 40-pin GPIO, makes this board ideal for interfacing between an ADC and computer [6]. A simplified schematic of the data acquisition system can be seen in Figure 2.

The device was programmed using the VHDL language within a *Quartus® II* workspace environment, with the design being split into several functional blocks to control each stage of the data acquisition process. The device operation begins by loading user-set values from RAM, including 'start' and 'stop' bits that allow the process to be controlled from the computer interface.

Accounting for a possible offset voltage in the tested system's equilibrium state, multiple reference measurements are made and averaged before initiating the impulse response. By subtracting the reference measurement from each sample, the impulse response is then centred about zero, simplifying the frequency analysis methods. Once this is complete, an impulse is initiated by driving a GPIO pin connected to a device that drives the impulse. The FPGA then begins to communicate with the ADC to initiate samples and read the conversion results.

### C. Computer Interface

The purpose of the computer interface is to allow the user full control over system parameters without requiring a full recompilation, while also displaying a systems impulse response in near real-time. In order to analyse and display the impulse response however, a reliable method for transferring the collected data from the FPGA is required. Fortunately, Altera provides a debugging application (*SignalTap® II Logic Analyzer*) designed to capture signals based on pre-defined triggers within the design [7]. The logic analyzer collects samples into a buffer, which once full, sends the data via JTAG communication to a *SignalTap* instance running on the host computer. Altera also provides a *MATLAB®* MEX function that allows *SignalTap* to acquire data directly into a matrix in the *MATLAB* environment. Given *MATLAB*'s ability in waveform analysis, this provides an excellent environment for both capture and analysis of impulse response data.

A Graphical User Interface (GUI) can be produced and operated using the facilities provided by *MATLAB*, giving the user a high degree of control over the device's operation. Other than setting parameters such as the sampling period and number of samples, the GUI also presents a number of additional options for running the device.

The first of these is the '*Reference Mode*' where, as mentioned previously, reference measurements from before the impulse response are subtracted from each sample if desired. The user is also able to select '*Continuous Mode*', where the impulse response is repeated after a set interval, allowing samples to be built up and averaged to increase the signal-to-noise ratio. Finally, the user can run the system in '*Increment Mode*'. Similar to continuous mode, the impulse response is repeated cyclically with the start of successive samples delayed by one clock pulse on each cycle. Given that the FPGA clock runs at 50 MHz, this allows samples to be built up with a period of 20 ns. By increasing the effective sampling frequency, a higher level of accuracy can be achieved in resolving the location of zero crossings in the signal. On top of all this, the user can also select which ADC channels are to be used in the analysis.

Once all the parameters have been selected, the device is started from within the GUI. In order to do this, *MATLAB* first creates a Memory Initialisation File (.mif) containing the RAM addresses and values for the updated parameters. Then, using Tool Command Language (Tcl) scripts and the *In-System Memory Content Editor* supplied by Altera, *MATLAB* uses the file to update the RAM within the device, including the 'start' bit for the data acquisition process [8]. Subsequently, functions controlling the *SignalTap* acquisition are called and the returned data is processed and displayed.

Some compatibility issues arise between 32-bit and 64-bit applications, restricting the software versions that can be used to operate this system. For the *MATLAB* MEX function to operate successfully, the software versions used were *Quartus II Web Edition 9.1 SP2 32-bit* and *MATLAB 2010a 32-bit*.

## III. Testing and Operation

As is standard practice for FPGA designs, test benches were produced for each section of code that verify their behaviour is as expected under all operating conditions. While this doesn't take into account the timing delays within the actual FPGA,

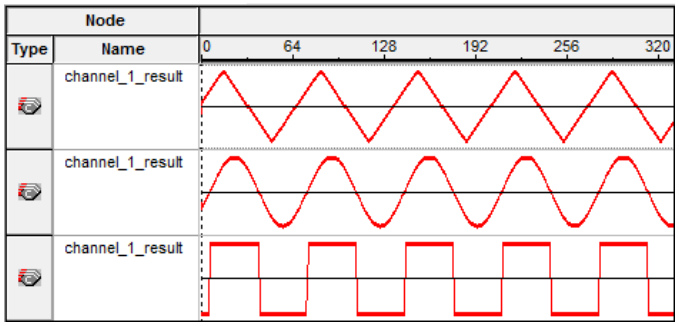


Fig. 3. Excerpt from the SignalTap II workspace during testing, demonstrating the results obtained when a triangular wave, sinusoidal wave, and square wave respectively, are used as inputs to the system.

the Register-transfer level (RTL) simulation ensures the design is logically correct. *ModelSim-Altera Starter Edition* was used as the RTL simulation tool for this design, aiding to debug each VHDL component. Once the design was verified, the data acquisition system was assembled for further testing.

The *SignalTap II Logic Analyzer* proved to be a valuable tool in the debugging process due to its ability to capture signals within the FPGA while running at full speed. This demonstrated that the FPGA was successfully communicating with the ADC, including the process of writing to the ADC's configuration register for channel selection.

The final testing stage incorporated the use of a function generator to test the linearity of the buffer stage and overall system behaviour. With the aid of an oscilloscope, the buffer output was found to accurately reproduce the entire $\pm 5$ V input range, whilst operating from a $\pm 6$ V power supply. The entire system was then subjected to a triangular wave input, covering a range of frequencies. In each case, the triangular wave was reproduced on the computer display for both channels, indicating that the full ADC range is functioning with no missing codes. This process was repeated using sinusoidal and square wave inputs, with the expected results being displayed in each case, as can be seen in Figure 3. Subsequent testing will use an electrical circuit consisting of a resistor, inductor, and capacitor (RLC) in series, to provide a transient second order response signal for analysis with the system.

## IV. Conclusion

This paper has discussed the various techniques used in designing, constructing, and testing a data acquisition system designed to capture the impulse response of a second order system. By incorporating a high-speed ADC and FPGA control with a computer interface, a comprehensive system has been produced for transient response analysis over a range of input magnitudes and frequencies. The GUI provides the user with a high degree of control over the systems operation and enables the near real-time display of a systems response.

## Acknowledgment

This work was performed in part at the Western Australian node of the Australian National Fabrication Facility, a company established under the National Collaborative Research Infrastructure Strategy to provide nano and micro-fabrication facilities for Australias researchers. This research was supported under a linkage grant by the Australian Research Council and by the Government of Western Australia Office of Science.

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