A High Deposition Rate Amorphous-Silicon Process for Use as a Thick Sacrificial Layer in Surface-Micromachining

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***Abstract*— Amorphous and polycrystalline silicon are commonly used as sacrificial layers in the surface micromachining of microelectromechanical systems (MEMS) devices, because they have high thickness uniformity over a large wafer area, and a similar coefficient of thermal expansion to suspended structural materials such as silicon nitride and silicon oxide. However, the low deposition rate of amorphous-silicon hinders its application in devices that require a suspension gap greater than several micrometres, and chemical stability can be an issue. This paper addresses these issues through the development of a high deposition rate hydrogenated amorphous silicon thin film process. We have demonstrated two unique processing regimes, which can support either a low or high temperature process. The low-temperature processes can be used to deposit silicon thin films at temperatures fromroom temperature up to 100°C, with deposition rates as high as 0.2 μm/min. The high-temperature recipes, deposited at temperatures at and above 200°C, have a slightly lower deposition rate of 0.14 μm/min, but are found to be chemically resistant to etching in positive photoresist developer. [2016-0273]**

***Index Terms*— Amorphous silicon, inductively coupled plasma chemical vapour deposition, microelectromechanical systems, sacrificial layer.**

I. Introduction

THE FABRICATION of application specific microelectromechanical systems (MEMS) utilising surface micromachining relies on the ability to select and use a variety of thin-film materials as the structural layer to achieve the desired electrical, mechanical and/or optical properties. For example, the structural layer of radio frequency (RF) MEMS switches can be made of nickel [1] or a dielectric material with aluminum electrodes [2], whereas MEMS chemical sensors typically use silicon/silicon nitride cantilevers or beams coated with a selective sensing layer [3], [4]. A crucial step in the fabrication of surface-MEMS is the release of a freestanding structure that relies on selective removal of the sacrificial layer underlying the structural layer [5]. The wide variety of structural materials require the availability of process compatible sacrificial materials and release processes with high etch-selectivity between the structural and sacrificial layers. In addition to process compatibility, the sacrificial layer must not negatively impact on the stress of the deposited structural layer in order to avoid unwanted deformation of the free standing structure [6], [7]. To achieve this, the sacrificial layer must be chemically stable, non out-gassing [8], and must match both the intrinsic stress and thermal expansion coefficient of any underlying and/or overlying materials.

Amorphous [9], polycrystalline [10] and single crystal silicon [11], and more recently porous-silicon [12], have all been used as thin film structural layers to create suspended structures. Amorphous silicon [13] and porous silicon [14], [15] can also be used as sacrificial layers, for example, in the surface-micromachining of CMOS compatible tuneable RF capacitors where the sacrificial layer is a sputtered amorphous silicon film [16]. An important requirement of sacrificial layers in certain applications is the ability to achieve large suspension gaps. In resonant operation, squeezed film damping limits the quality factor, thus requiring either high vacuum or suspension gaps greater than 10 μm [17]. For bio-sensing applications, where sensing requires infiltration of cells of up to 10 μm in size, large gaps are also required [18]. However, the low deposition rate of amorphous silicon makes it extremely time consuming to achieve large release gaps greater than several micrometres, and the chemical stability of both amorphous and porous films can be an issue.

This work presents a process for high deposition rate amorphous silicon for use as a thick sacrificial layer, using an inductively coupled plasma chemical vapour deposition (ICPCVD) process with a heated substrate. A significant advantage of this process is the high deposition rate (>120 nm/min), which is higher than previously reported ICPCVD processes (up to 90 nm/min) [19]–[23]. However, it is possible to achieve significantly higher deposition rates using microwave chemical vapour deposition processes (MWCVD),

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TABLE I

PROCESS STEPS IN THE SILICON DEPOSITION RECIPE [APC VALVE = AUTOMATIC PRESSURE CONTROL VALVE, WHICH CAN BE SET IN THE RANGE OF 0 – 100%; RF POWER = POWER OF THE RF GENERATOR DRIVING THE HEATED TABLE; ICP POWER = POWER OF THE RF GENERATOR DRIVING INDUCTIVELY COUPLED ANTENNA]

Step name		SiH_4 flow	Ar flow	Chamber pressure	APC valve	RF power	ICP power	Time
1:	Temperature stabilization	0 sccm	0 sccm	0 mTorr	OPEN	0 W	0 W	30 min.
2:	Gas flow	30 sccm	30 sccm	12 mTorr	48 %	0 W	0 W	30 sec.
3:	Plasma strike, phase 1	30 sccm	30 sccm	12 mTorr	48 %	10 W	50 W	5 sec.
	Plasma strike, phase 2	30 sccm	0 sccm	5 mTorr	OPEN	10 W	150 W	2 sec
	Plasma strike, phase 3	30 sccm	0 sccm	5 mTorr	OPEN	0 W	200 W	2 sec
4:	Silicon deposition	30 sccm	0 sccm	5 mTorr	OPEN	0 W	300 W	30 min.

up to 380 nm/min [24], [25], or hot wire chemical vapour deposition (HWCVD), up to 780 nm/min [26]. But these alternative processes require deposition temperature of at least 250 °C. The high deposition rate enables deposition of nominally 10 μm thick sacrificial layers within 2 hours, which is well within the typical processing times for surface-MEMS structures containing multiple layers. The proposed silicon sacrificial layer is ideal for fabrication of MEMS devices on small samples, where spin-coating techniques for sacrificial layers tend to produce a significant edge bead which cannot be easily removed. In addition, MEMS devices fabricated with a thick ICPCVD silicon sacrificial layer can be released using simple wet chemical etching in tetramethyl ammonium hydroxide (TMAH) or potassium hydroxide (KOH) solutions, as well as using dry etching via XeF_2 vapour [27]–[29] or SF_6 plasma [30]. The variety of release methods, which can be used with the proposed sacrificial layer material, allows high selectivity to most modern structural layer materials including silicon oxide, silicon nitride and most metals.

II. DEPOSITION PROCESS

The deposition of amorphous silicon thin films was performed using an Oxford Instruments Plasmalab System 80+, which uses two 13.56 MHz RF generators. The deposition recipe is shown in Table I and contains four main steps. The process commences with temperature stabilization of the sample (30 min) followed by a gas flow step (30 sec) to stabilize the chamber pressure and gas composition. Two gasses are metered into the chamber; SiH_4 is delivered through a bottom gas ring while argon is delivered through a gas shower above the ICP antenna, as depicted in Fig. 1(a). Argon is used to assist in striking the plasma and is switched off during deposition [31]. A 3-phase plasma strike procedure is required to start and stabilize the low-pressure pure silane plasma.

During deposition, the ion energy (DC bias) depends on the RF generator power connected to the heated table, whereas the ion current (plasma density) is controlled by the RF generator power connected to the inductively coupled antenna [32]. During the main stage of the silicon deposition, only one RF generator was used, with the RF generator connected to the heated table being switched off to minimize the ion energy,

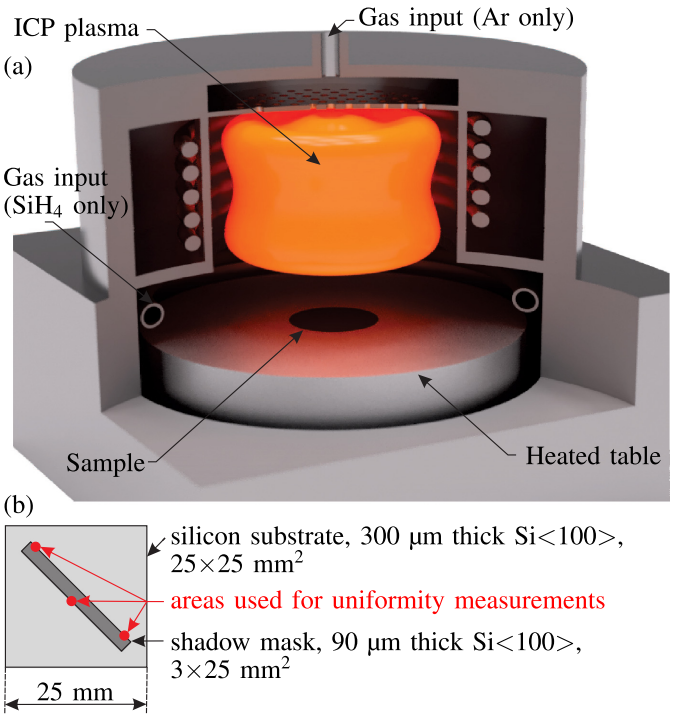

Fig. 1. (a) Schematic view of Oxford Instruments Plasmalab System 80+ deposition chamber, (b) The adopted general arrangement of the test sample with 90 μm thick silicon shadow mask and marked points for measurements of thickness uniformity of film deposited on the 25×25 mm^2 underlying silicon sample area.

since low ion energy helps in avoiding formation of thin films with significant in-build compressive stress. The high deposition rate can be obtained by adjusting a few variables: gas composition, ICP power, and power to the RF generator connected to the heated table (DC bias). To achieve high deposition rate, we maximize the ICP power [33] and minimize the RF power connected to the heated table (DC bias) [34]. For this experiment, we used the maximum value of ICP power and the maximum flow of SiH_4 available in the tool in order to maximize deposition rate [35].

All depositions were conducted on 300 μm thick, 25 × 25 mm^2 silicon ⟨100⟩ substrates coated with a 100 nm thick SiO_x film, which was used to separate the deposited silicon from the substrate. Before deposition, a 90 μm thick

strip of silicon was placed on the substrate as a shadow mask (Fig. 1(b)). The resulting step in the film deposited on the 300 μm thick substrate was used to measure the thickness of the layer, and the 90 μm thick silicon strip with the deposited film was used for stress measurement of the deposited silicon film via stress induced substrate curvature [36]. All depositions were of 30 min duration. In order to investigate the effect of substrate temperature on the film properties, the heated table temperature was controlled to a fixed value between 25 °C and 300 °C during deposition.

III. Results and Discussion

The deposited silicon thin films were characterized to assess material parameters relevant to the film being used as a sacrificial layer. The properties to be evaluated included deposition rate, film thickness and uniformity, stress, Young's modulus, hardness, surface roughness and chemical resistance to positive photoresist developer. In all cases, no visible defects were observed in the deposited thin films using optical microscopy. As the proposed recipe is intended to be used as a thin film for sacrificial layers in MEMS devices, the void density of the deposited films was not extensively investigated.

A. Deposition Rate and Thickness Uniformity

Film thickness (ranging from 4 μm to 6 μm) was measured using a Veeco Dektak 150 stylus profilometer. Measurements were made in three regions, distributed over the area of the 25 $\times$ 25 mm^2 sample as indicated in Fig. 1(b), and used to assess both deposition rate and thickness uniformity. These parameters are shown in Fig. 2(a,b) as a function of deposition temperature, where the average deposition rate is seen to monotonically decrease with increasing substrate temperature from a value of 201 nm/min observed for the film deposited at 25 °C to 129 nm/min for the film deposited at 300 °C, as shown in Fig. 2(a). It is a common observation for low pressure ICPCVD processes in this temperature range that as the deposition temperature increases the film density also increases. This can explain the noticeable decrease in deposition rate with increasing substrate temperature, given that the deposition process is consuming a similar amount of silicon radicals at all deposition temperatures, but results in progressively denser, and therefore thinner layers with increasing deposition temperature. Similar behaviour has been observed previously by Nominanda *et al.* [37] and Jeong *et al.* [38] for plasma enhanced chemical vapour deposition (PECVD) processes.

In the low-temperature regime below 100 °C, thickness variation decreased with increasing temperature and was measured via Dektak to always be better than ±1.09%. An abrupt change in thickness uniformity is observed at a substrate deposition temperature of 150 °C and, as such, we use this temperature to define the transition from a low-temperature process to a high temperature process. Low-temperature recipes produced silicon thin films that could be etched in positive photoresist developer and achieved high deposition rates, allowing a 15 μm thick sacrificial layer to be deposited in 75 minutes at 25 °C. High-temperature recipes produced silicon films that were stable in positive photoresist developer but with lower

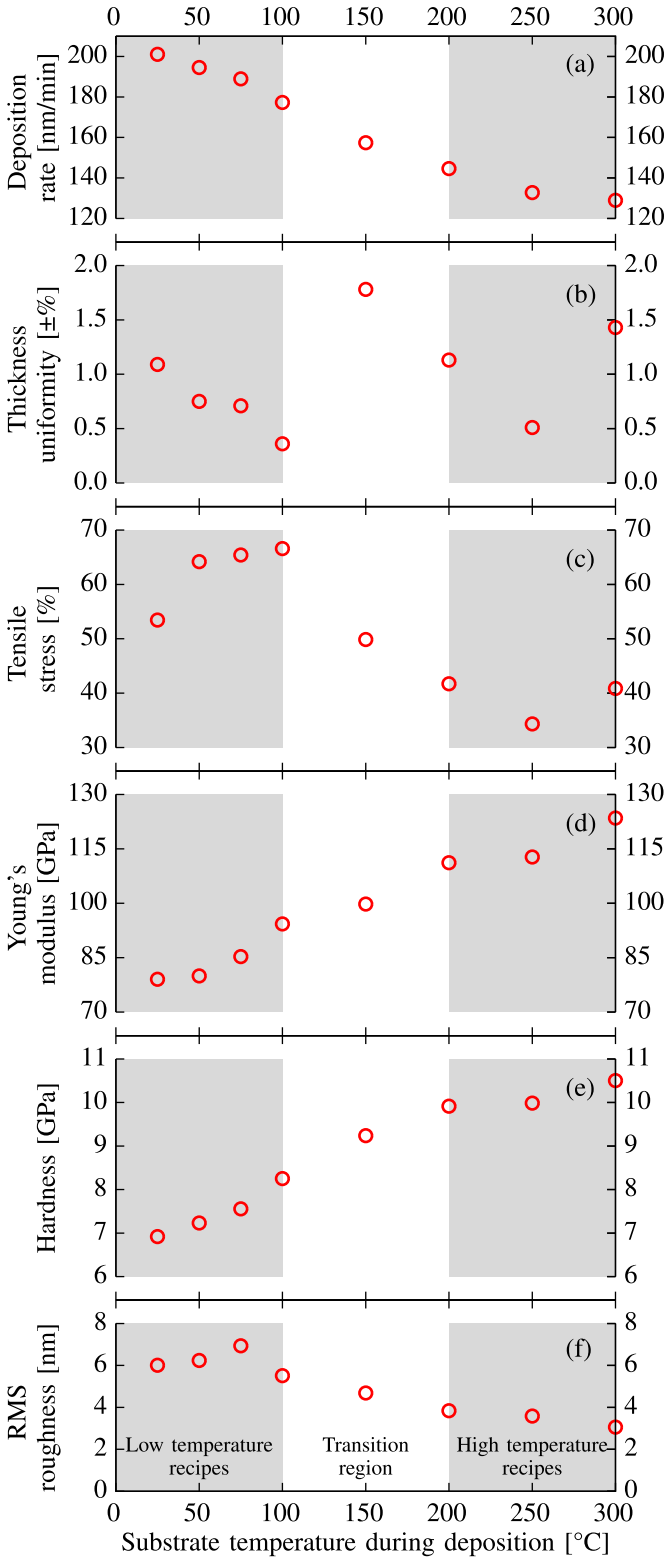

Fig. 2. Thin film (a) deposition rate, (b) thickness uniformity, (c) stress estimation, (d) Young's modulus, (e) hardness, and (f) RMS surface roughness for amorphous silicon as a function of substrate temperature during deposition.

deposition rates, requiring 2 hours to achieve the same 15 μm thick sacrificial layer at 300 °C. Relative to all other deposited films, the film thickness variation for 150 °C depositions was found to be the highest (±1.78%) and was consistently lower

for thin films deposited above 150 °C. The reported change in the thickness uniformity is as we observed in our measured data (one sample, three separate measurements). The variation of the thickness is within the specification of the tool of <6% over a 2" diameter sample. This change may not be fully associated with the change in deposition temperature but may also reflect tool variation.

The ICPCVD silicon deposition process can be limited by surface-reactions [5] and/or by the density of available radicals in the plasma [39]. For a process that is limited by surface-reactions excess radicals are present in the chamber which can result in the formation of powder-like polymerized disilane (SiH_2) particles [39]. This is a common observation for higher pressure silicon deposition processes [40]. The deposition recipes investigated in this work were specifically chosen so as to avoid powder formation within the chamber, suggesting that the deposition rates were limited by the available radicals in the plasma. Once the process conditions were achieved that did not result in powder formation in the chamber, the density of available radicals in the plasma was kept constant by ensuring the pressure, gas flow, and RF power were all kept constant.

B. Thin Film Stress Estimation

In many applications, the stress of released thin films needs to be minimized. This necessitates matching the stress of the sacrificial layer and the structural thin film allowing the deformation of any free standing structures to be minimized during the release process [6], [7].

The stress of thin film amorphous silicon layers studied in this work was estimated using thin film stress induced substrate bending and Stoney's formula [36]. The curvatures of the 90 μm thick silicon strips with dimensions of 3×25 mm^2 were measured before and after depositions of the amorphous silicon thin films using a Zygo NewView white light optical surface profilometer. Figure 2(c) shows the resulting stress estimation as a function of substrate deposition temperature. It should be noted that in all cases a relatively low value of intrinsic tensile stress was found (<70 MPa). Not only is tensile stress preferred over compressive stress whenever it is desirable to create flat suspended beams and plates, but the observed magnitude of the stress is considerably lower than for hydrogenated amorphous silicon films deposited using PECVD or RF glow discharge. Yin *et al.* [41] reported compressive stress values in the range from 300 MPa to 800 MPa for hydrogenated amorphous silicon prepared via plasma-enhanced chemical vapour deposition (PECVD). Harbison *et al.* [42] reported compressive stress values in the range from 50 MPa to 800 MPa for hydrogenated amorphous silicon thin films deposited using RF glow discharge.

C. Young's Modulus and Hardness

The Young's modulus and indentation hardness of the samples were estimated via the nanoindentation technique [43] using a Hysitron TI 950 TriboIndenter instrument and a Berkovich indentation tip [44]. Each amorphous silicon thin film sample was indented with 5 sets of 30 indents with loading progressively increasing from 0.5 mN to 10 mN. The Young's modulus and hardness of the material were calculated using the Oliver and Pharr method [45], where the penetration depth exceeded 50 nm [46], [47]. During the calculations we assumed $\nu_{\text{silicon}} = 0.278$ [48], $\nu_{\text{indenter}} = 0.07$, and $E_{\text{indenter}} = 1140$ GPa [46]. The obtained Young's modulus and hardness values are shown in Fig. 2(d,e) as a function of substrate deposition temperature.

The generally high Young's modulus and hardness values observed, especially for deposition at the highest temperature (300 °C), are comparable with values reported in the literature for high quality thin film silicon layers. Jiang *et al.* [49] reported values of Young's modulus up to 100 GPa and hardness up to 10 GPa for sputtered amorphous hydrogenated silicon. In comparison, Bhushan *et al.* [50] measured a Young's modulus of 179 GPa and a hardness for undoped crystalline silicon ⟨100⟩ of 13 GPa.

D. Surface Roughness

The root-mean-squared (RMS) surface roughness of the samples was calculated from 5×5 μm^2 surface profile images of the silicon films acquired using a WITec alpha 300RA+ atomic force microscope (AFM), and calculated using WITec Project FOUR software, version 4.0. Figure 3 shows the AFM images of the amorphous silicon thin film surfaces obtained for films prepared at the investigated deposition temperatures, and the RMS surface roughness values are shown in Fig. 2(f) as a function of deposition temperature. The surface roughness was found to decrease with increasing substrate deposition temperature, with the highest surface roughness (6.9 nm) observed for a deposition temperature of 75 °C, and the lowest value (3.1 nm) occurred for a substrate temperature of 300 °C. The results indicate that more robust films (lower RMS surface roughness, higher Young's modulus and higher indentation hardness) are formed at higher substrate deposition temperatures. For use as a sacrificial layer, the most important parameter can often be the RMS surface roughness, since any subsequently deposited layers will conform to the same degree of roughness [51]. Thus, the surface roughness needs to be minimized, especially for MEMS optical surfaces, in order to achieve adequate performance. For optical MEMS, the maximum acceptable level of surface roughness is often given as $\lambda/20$ [52]–[56]. For example, for devices operating at a wavelength of 1550 nm, the surface roughness value needs to be <78 nm. Surface roughness values observed in this study are significantly below this limit.

E. Chemical Resistance to Positive Photoresist Developer

The amorphous silicon thin films deposited at low temperatures were found to be readily etched in a positive photoresist developer. Chemical resistance to positive photoresist developer is important if any subsequent photolithography process is required to be undertaken directly on the sacrificial layer. Chemical resistance to developer was determined by immersing samples in Microchem AZ326, an aqueous solution of 2.38% TMAH. Initially, samples were immersed in the

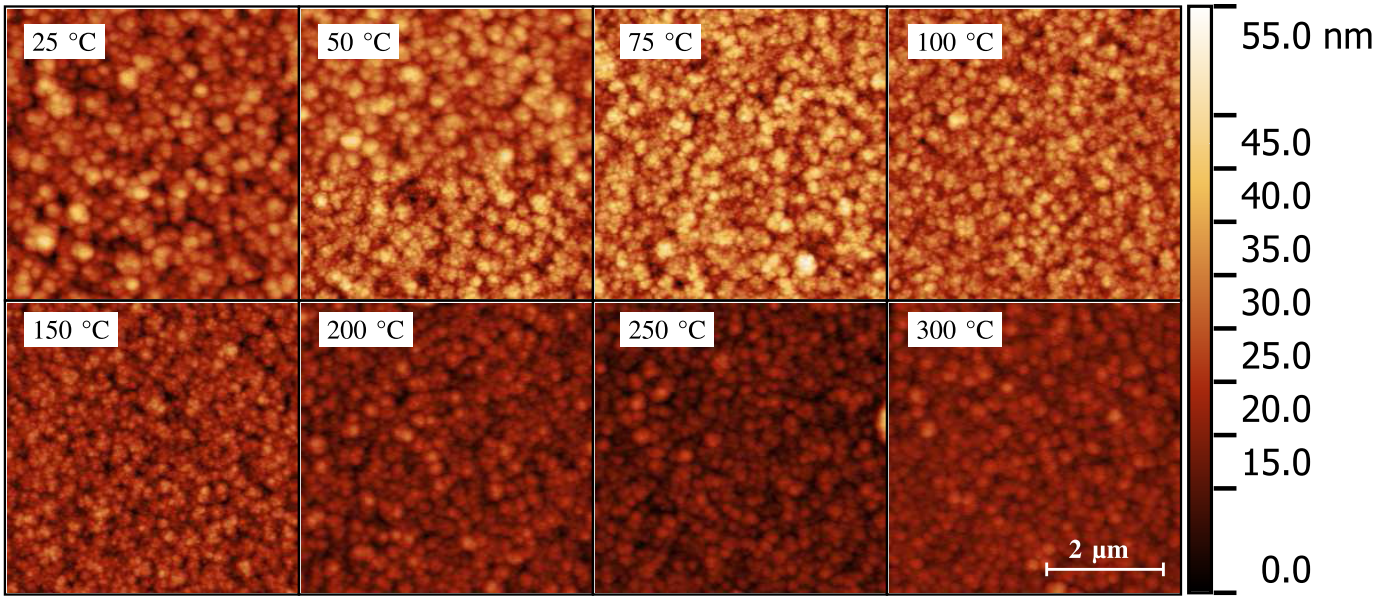

Fig. 3. AFM images of surfaces of amorphous silicon thin films deposited at different substrate temperatures. The indicated scales are common to all images.

developer for 5 minutes, and the thickness change of the amorphous silicon layer was measured using a Veeco Dektak 150 stylus profilometer. Next, the immersion was repeated twice, each time for an additional 10 minutes. The amorphous silicon samples deposited at temperatures up to 100 °C were found to be completely etched away during the first 5 minute immersion. The sample with a deposition temperature of 150 °C was partially etched over the same 5-minute duration, and had a resulting rough surface. In contrast, amorphous silicon samples deposited at temperatures of 200 °C and above were found to be chemically stable and not etched in positive photoresist developer, even after a total immersion time of 30 minutes. Not surprisingly, samples with higher hardness were found to be more resistant to etching in positive photoresist developer.

It was found by Haller *et al.* [57] that hydrogenated amorphous silicon etch rate can be directly and positively correlated with hydrogen content in deposited material. It is expected that total hydrogen content in films deposited at lower temperatures (up to 100 °C) is significantly higher in comparison to films deposited at 150 °C and above. Moravej *et al.* [58] reported a change from 6.0 at% to 3.0 at% total hydrogen content in amorphous silicon thin films for a deposition temperature change from 100 °C to 150 °C; and the hydrogen content in films prepared in the temperature range from 25 °C to 100 °C is expected to be even larger. For temperatures above 150 °C, Moravej *et al.* [58] found that the density of the films increases significantly as the deposition temperature is increased, and this may be due to a decrease in hydrogen content in the form of SiH_2 with increasing deposition temperature. Based on this, we correlate the expected excessive hydrogen concentration of films deposited in the low temperature regime with their ability to be etched in positive photoresist developer.

It was found by Jiang *et al.* [49] that hydrogen content in silicon thin films can be directly correlated with Young's modulus and indentation hardness. That can be further explained by the work of Moravej *et al.* [58], who reported that films deposited at lower temperatures contain a significantly higher void density. The presence of voids can imply the lower values of both Young's modulus and indentation hardness observed for films deposited in low deposition temperature regime as compared to high deposition temperature regime. A summary of all the experimental results along with the observed film chemical resistance are tabulated in Table II, and compared to selected literature reports for high quality silicon films. These results confirm the high quality of the silicon thin films developed in the course of this study.

F. Example of Fabricated Structures Using Amorphous Silicon as a Sacrificial Layer

To demonstrate the use of the developed process recipes in surface micromachining, test micro-structures were fabricated and investigated. The test devices were fabricated using a silicon nitride/gold structural thin film bilayer and a high-temperature amorphous silicon sacrificial layer. Structures were fabricated on a silicon substrate wafer covered with 100 nm thick SiO_x, and 50 nm thick gold metal pads were deposited for electrostatic actuation of fabricated devices. A 6 μm thick amorphous silicon sacrificial layer was deposited at a temperature of 300 °C to minimize surface roughness. We tested depositions up to 1 hour long, creating 12 μm thick films. The deposition rate was constant in these tests and did not change with time. Subsequently, the sacrificial layer was patterned using reactive-ion etching (RIE). On top of the sacrificial layer a 50 nm thick film of gold and 700 nm thick film of SiN_x were deposited and patterned to form the structural layer.

All of the amorphous silicon thin films investigated in this work can be etched by using dry chemical etching in XeF_2 vapour, with etch rates up to 2 μm/min in the vertical direction

TABLE II
SUMMARY OF THE MEASURED MATERIAL PROPERTIES FOR ICPCVD SILICON THIN FILMS PREPARED USING LOW- AND HIGH-TEMPERATURE RECIPES

	Low temperature recipe (25 °C – 100 °C)	**High-temperature recipe (200 °C – 300 °C)**	**Comparison with literature reports**	
			Deposition technique	**Reported values**
Deposition rate [nm/min]	177 – 201	128 – 144	ICPCVD [19] ICPCVD [20] ICPCVD [21] ICPCVD [22] ICPCVD [23] MWCVD [24] MWCVD [25] HWCVD [26]	60 – 75 nm/min [19] ~36 nm/min [20] 36 – 84 nm/min [21] 90 nm/min [22] 65 nm/min [23] 282 nm/min [24] 380 nm/min [25] 780 nm/min [26]
Thickness uniformity [±%]	0.36 – 1.09	0.51 – 1.43	ICPCVD [59]	±6% over 50 nm area [59]
Thin film tensile stress [MPa]	54 – 67	34 – 42	PECVD [41] RF glow discharge CVD [42]	compressive: 300 – 800 MPa [41] 50 – 800 MPa [42]
Young's modulus [GPa]	79 – 94	111 – 123	low pressure CVD [49]	up to 100 GPa [49]
Indentation hardness [GPa]	6.9 – 8.3	9.9 – 10.5	low pressure CVD [49]	up to 10 GPa [49]
RMS surface roughness [nm]	5.5 – 6.9	3.1 – 3.8	–	–
Chemical resistance to positive photoresist developer	No	Yes	–	–

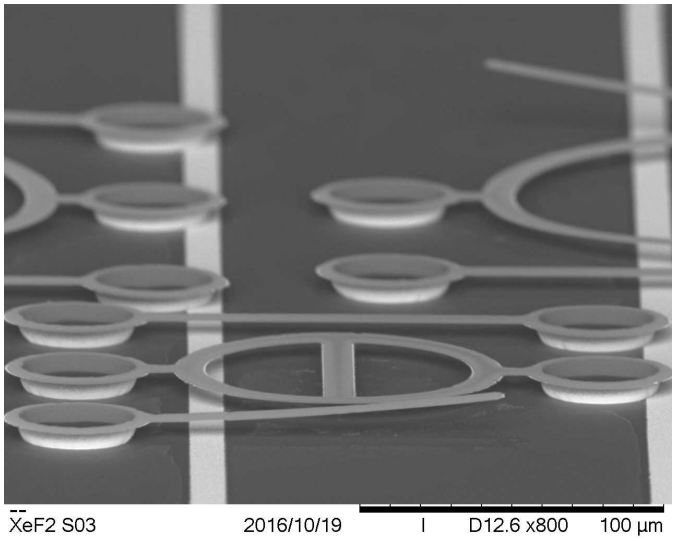

Fig. 4. SEM image of released micro-structures using silicon as the sacrificial layer (cantilevers, double-supported beams and Guckel rings) suspended 6 μm above the substrate. The silicon nitride/gold structures are fabricated on silicon oxide coated substrate and released using chemical dry etching in XeF_2 vapour.

and up to 4 μm/min in the horizontal direction [27]–[29], SF_6 plasma with etch rates up to 15 μm/min [30], or heavily concentrated and heated TMAH and KOH solutions, with etch rates up to 1.4 μm/min (e.g., Tabata *et al.* [60] used a solution of 22 wt% TMAH at 90 °C, and Shikida *et al.* [61] used a solution of 34.0 wt% KOH at 71 °C). In our studies, the fabricated structures were released using chemical dry etching in XeF_2 vapour. The test structures included cantilevers and double-supported beams with dimensions of 10 μm × 220 μm. Guckel rings were also fabricated with diameter ranging from 90 μm to 210 μm with a beam width of 10 μm as shown in Fig. 4. The release process using XeF_2 etching took less than 5 minutes for the fabricated structures.

IV. CONCLUSIONS

We have demonstrated high quality amorphous silicon thin films deposited with high deposition rates using an ICPCVD process, which readily allows control over material properties important for micromachining of MEMS structures. All deposited films can be used for optical MEMS due to the low RMS surface roughness. The achieved low tensile stress (<70 MPa) is an initial requirement in order to minimize the influence of the sacrificial layer on subsequently-deposited structural materials. We achieved a high thickness uniformity ranging from ±0.36% to ±1.78% across the full deposition temperature range of 25 °C to 300 °C. Overall, the achieved material parameters allow the use of the investigated films as a sacrificial layer for fabrication of MEMS devices, especially in situations where a suspension gap greater than several micrometers is a necessary requirement.

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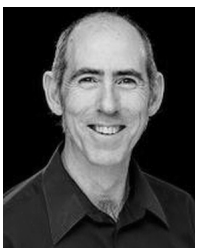

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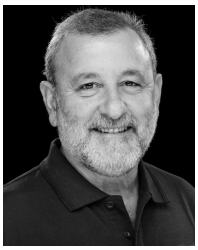

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